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KRAMER & AMADO, P.C.
Suite 240
1725 Duke Street
Alexandria, VA 22314

EXAMINER	
NGUYEN, HOA CAO	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALEX L. CHAN,
PAUL BROWN, and CHARLES M. ELLIOTT

Appeal 2009-004577
Application 10/761,343
Technology Center 2800

Decided: September 18, 2009

Before BRADLEY R. GARRIS, PETER F. KRATZ, and
MARK NAGUMO, *Administrative Patent Judges*.

NAGUMO, *Administrative Patent Judge*.

DECISION ON APPEAL

A. Introduction[1]

Alex L. Chan, Paul Brown, and Charles M. Elliott ("Chan") timely appeal under 35 U.S.C. § 134(a) from the final rejection[2] of claims 1-4 and 9-12. We have jurisdiction under 35 U.S.C. § 6. We AFFIRM.

The subject matter on appeal relates to a printed wiring board ("PWB") having conductive passages through the board (plated through hole ("PTH") "vias") and conductive connection pads for making contact with the ball grid arrays ("BGA") of solder that have largely replaced conductive pins on the underside of modern integrated circuit chips. The claimed invention provides for regions free of vias where capacitors may be connected without obstructing vias and connections to the vias. The capacitors are commonly used to bridge the input and return lines of the power supply, thereby decoupling the power supply from the IC chips. The absence of vias is said to be compensated by providing "shared vias" adjacent to the missing vias.

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[1] Application 10/761,343, *Shared Via Decoupling for Area Arrays Components*, filed 22 January 2004. The specification is referred to as the "343 Specification," and is cited as "Spec." The real party in interest is listed as ALCATEL. (Appeal Brief, filed 21 April 2008 ("Br."), 1.)

[2] Office action mailed 4 December 2007 ("Final Rejection"; cited as "FR"). The Examiner subsequently withdrew the rejection of claims 5 and 6, which currently stand objected to as being dependent on rejected claim 2, but are otherwise said to be allowable. Claims 7 and 8 were canceled. Claim 13, the only other pending claim, has been withdrawn from consideration.

Representative Claims 2, 9, and 10 are reproduced from the Claims Appendix to the Principal Brief on Appeal:

2. A printed wiring board (PWB) for mounting a high performance integrated circuit, comprising:

on a top side of said PWB, a modified via array with BGA columns and BGA rows of ball connection pads;

a modified vias array of plated through hole (PTH) vias,

with each via column Col(n) arranged between two respective BGA columns c(n) and c(n+1) and

each via row R(k) arranged between two respective BGA rows r(k) and r(k-1),

wherein 2m vias of said via column Col(i) placed in successive via rows R(j) to R(j+2m-1) of said modified vias array are depopulated to obtain a free space on the back side of said PWB,

wherein 2m corresponding vias in a via column Col(i+1) adjacent to said via column Col(i) and placed in successive via rows R(j) to R(j+2m-1) of said vias arrays are shared vias, and

wherein $n \geq 1$, $k \geq 2$, $2 \leq i < n$ and $j < k$.

(Claims App., Br. 8-9; indentation and paragraphing added.)

9. The PWB of claim 2, wherein

a first shared via in said via column Col(i) and said via row R(j) provides a power contact

to a first associated *ball contact pad* in said *via* column c(i) and said *via* row r(j+1) and

to a second associated *ball contact pad* in said *via* column c(i+1) and said *via* row r(j).

(Claims App., Br. 10; indentation, paragraphing, and emphasis added.)

10. The PWB of claim 9, wherein

> a second shared via in said via column Col(i) and said via row R(j+1) provides a ground contact
>
> > to a third associated *ball contact pad* in said *c(i)* and said *via* row r(j+2) and
> >
> > to a fourth associated *ball contact pad* in said *via* column c(i+1) and a *via* row r(j+1).

(Claims App., Br. 10; indentation, paragraphing, and emphasis added.)

The Examiner has maintained the following grounds of rejection:[3]

> A. Claims 9 and 10 stand rejected under 35 U.S.C. § 112(2).
>
> B. Claims 1-4 stand rejected under 35 U.S.C. § 102(e) in view of the teachings of Clarkson.[4]
>
> C. Claims 11 and 12 stand rejected under 35 U.S.C. § 103(a) in view of the teachings of Clarkson.

Chan contends that claims 11 and 12 have been rejected as indefinite based on the rejection of claim 2 for indefiniteness, which has been amended "exactly as suggested in the [final] rejection" (Br. 4). Therefore, Chan argues, the rejection of claims 11 and 12 as indefinite should be withdrawn.

The Examiner responds that claim 9 refers to shared vias "in said via column Col(i)," whereas claim 2 specifies that via column Col(i) is depopulated of vias. (Ans. 3-4; cf. FR 3-4, which especially carefully uses Chan's nomenclature for via columns and rows (via column Col(n) and

[3] Examiner's Answer mailed 10 July 2008. ("Ans.").

[4] Robert Roy Clarkson and Glen Robert Harding, *Printed Circuit Board having a Microelectronic Semiconductor device Mount Area for Trace Routing Therethrough*, U.S. Patent Application Publication US 2003/0043560 A1 (6 March 2003).

via row R(k)) and for BGA columns and rows (BGA column c(n) and BGA row r(k)) (here, we use the indices (n and k) arbitrarily).) The Examiner analyzes claim 9, makes some assumptions about what the indices should be for [ball] contact pads, and determines that "there is an error in such arrangement of pads; because with this arrangement, for each power via there is at least one pad formed 3 rows down from its connected via and *this [is] not what [is] described in the Specification*." (Ans. 4; emphasis added.) The Examiner reports on an attempted fix for the "error," but determines that "this will lead to the same structure as shown in claims 5-6." (*Id.* at 4-5.) The Examiner concludes that the structure intended to be claimed cannot be determined, and withdraws the claim from consideration as against the prior art. (*Id.* at 5.)

As for the rejections in view of Clarkson, Chan submits "that Clarkson does not disclose, teach or suggest, shared vias according to the combinations recited in independent claims 1 and 2." (Br. 5.) For that reason, the rejections of the remaining claims, all of which depend from claim 2, are said to be improper. Chan does not explain why the vias described by Clarkson are not "shared vias," nor does Chan explain what "combinations" recited in the claims are not met by any shared vias that might be present.

The Examiner finds that Clarkson describes an array of modified vias (round structures in Clarkson Figure 2A) and an offset array of BGA connection pads (square structures in Clarkson Figure 2A), in which a column of vias (135 in Clarkson Figure 2A) and a row of vias (130 in Clarkson Figure 2A) have been removed. (FR 5-6.) The Examiner finds

that Clarkson describes through-hole vias in paragraph 18 (*id.*), and shared vias in paragraph 30 (*id.* at 6).

B. Findings of Fact

Findings of fact throughout this Opinion are supported by a preponderance of the evidence of record.

The 343 Specification

1. The 343 Specification establishes a distinct nomenclature for the columns and rows of the ball grid array (BGA) and the modified vias array. (Spec. 5, ¶ [0021] and 10, ¶ [0039].)

2. According to the 343 Specification, "each via column Col(n) [is] arranged between two respective BGA columns c(n) and c(n+1) and each via row R(k) [is] arranged between two respective BGA rows r(k) and r(k+1)." (Spec. 5, ¶ [0021].)

3. Thus, via columns and rows are denoted by upper case labels, Col(n) and R(k), respectively, while ball contact pad columns and rows are denoted by lower case labels, c(n) and r(k), respectively.

4. Importantly, the via array is offset from the BGA contact array, such that via columns and rows do not contain BGA contacts, and BGA contact columns and rows do not contain vias.

5. We note in passing that the convention adopted for labeling BGA rows in appealed claim 2 differs from the convention set out in the 343 Specification.

6. The term "shared via" occurs frequently throughout the 343 Specification, but is not explicitly defined.

7. For example, according to the 343 Specification, an object of the invention is to "provide a decoupling solution that leverages the shared via arrangement being used on a growing number of BGA devices." (Spec. 5, ¶ [0019].)

8. The 343 Specification describes "routing channels" that are said to be "obtained between two columns (or two rows) of vias, by changing the angle of the pad in two of the adjacent rows. . . . [t]he channel is used, as the name indicates, for routing traces from the vias in the core of the array." (Spec. 4, ¶ [0016].)

9. The 343 Specification also teaches that the modified vias array of the present invention involves replacing "at least a portion of one column or row of the vias" by "respective shared vias in an adjacent row, and the shared vias have been connected to either a power supply or a power return." (Spec. 5, ¶ [0020].)

10. The 343 Specification goes on to explain that decoupling capacitors "can be electrically connected across the via pads to decouple the power supply and the power return at the two adjacent vias." (Spec. 5, ¶ [0020].)

Clarkson

11. Clarkson describes "an optimal microelectronic semiconductor device mount area on a printed circuit board." (Clarkson 1, ¶ [0010].)

12. According to Clarkson, "[t]he optimal mount area includes a plurality of collinear arrangements of attach pads and collinear arrangements of vias so that . . . at least one signal trace may be routed directly through the mount area." (Clarkson 1, ¶ [0010].)

13. Moreover, Clarkson teaches that "capacitors may be coupled directly within the mount area on [the] bottom surface of the printed circuit board." (Clarkson 1, ¶ [0010].)

14. Clarkson also describes "clearance vias" that pass completely through a PCB "to provide routing for adjacent source voltage pads or ground pads." (Clarkson 2, ¶ [0018].)

15. According to Clarkson, "[b]y using clearance vias, a single source voltage pad can be used to provide a voltage source for all layers of a multi-layered PCB." (Clarkson 2, ¶ [0018].)

16. In the Figures, Clarkson depicts vias by round discs and attach pads by squares. (Clarkson 2, ¶ [0021], describing Figure 1.)

17. Connections between vias and attach pads, or between vias and vias, for example, are shown by traces between the elements, as shown in Figures 4A and 4B.

18. Referring to Figure 4A, shown right, Clarkson describes how mount areas 400 are created with horizontally oriented channel 330 and vertically oriented channel 335 by the omission of an intermediate row and column of vias "and respectively replacing them along the peripheral row and column of attach pads." (Clarkson, 3, ¶ [0030].)

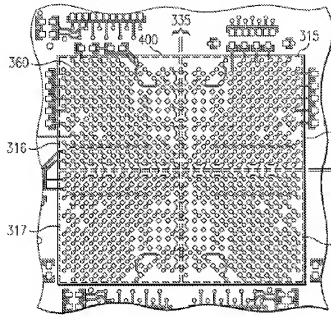

FIG. 4A

19. Clarkson teaches that "[g]round and power vias can advantageously be located adjacent to channels 330 and 335." (Clarkson, 3, ¶ [0030].)

{Figure 4A shows a top view of a printed circuit board}

C. Discussion

As the Appellant, Chan bears the procedural burden of showing harmful error in the Examiner's rejections. *See, e.g., Gechter v. Davidson*, 116 F.3d 1454, 1460 (Fed. Cir. 1997) ("[W]e expect that the Board's anticipation analysis be conducted on a limitation by limitation basis, with specific fact findings for each *contested* limitation and satisfactory explanations for such findings.") (emphasis added.) Arguments not timely presented are waived. 37 C.F.R. § 41.37(c)(1)(vii) (2009).

As indicated by the Examiner, claims 9 and 10 present several interpretive problems that arise out of the labeling system adopted by Chan in the 343 Specification.

According to the 343 Specification, vias are arranged in columns and rows designated by "Col(n)" and "R(k)," respectively (emphasis added), i.e., by labels beginning with uppercase letters. Similarly, BGA contact pads are arranged in columns and rows, designated, in contrast, by "c(n)" and "r(k)," respectively, i.e., by labels beginning with lowercase letters. Moreover, via columns and rows do not contain BGA contact pads, and vice-versa. (Spec. 5, ¶ [0021].) The 343 Specification emphasizes this point by referring to a separate vias array and a separate modified ball grid array, and by referring to "via column Col(n)," "via row R(k)," and to "BGA column c(n)" and "BGA row r(k)" in the description at page 5, ¶ [0021]) and at pages 10-11, ¶¶ [0039]-[0040].

Claims 9 and 10 refer to a "ball contact pad" in "*via* column c(i)" and "*via* row r(j+1)" (emphasis added). However, ball contact pads are not, according to the 343 Specification, in via rows or columns. (Spec. 5, ¶ [0021].)

The interpretive difficulties continue with the relation between via columns and BGA columns, and between via rows and BGA rows. Again, the 343 Specification states that "each via column Col(n) [is] arranged between two respective BGA columns c(n) and c(n+1)," while "each via row R(k) [is] arranged between two respective BGA rows r(k) and r(k+1)." (Spec. 5, ¶ [0021].) In contrast, claim 1 requires that the via row R(k) be between BGA contact rows r(k) and r(k-1).

The consequences of these definitions as to the definiteness, *vel non*, of claims 9 and 10, however, differ. As the Examiner recognized, as evidenced by the care with which the statement of rejection uses Chan's uppercase/lowercase nomenclature for vias versus BGA columns and rows, claims 9 and 10 require BGA contact pads to be in via columns and rows, where BGA contacts do not exist, according to the 343 Specification. The plain language of the claims requires an impossibility: therefore, the claims are indefinite. *Cf. Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357 (Fed. Cir. 1999):

> where as here, claims are susceptible to only one reasonable interpretation and that interpretation results in a nonsensical construction of the claim as a whole, the claim must be invalidated, thus preventing unduly burdening competitors who must determine the scope of the claimed invention based on an erroneously drafted claim.

The appealed claims are in an application: they are not patented, and no presumption of validity attaches to them. The Examiner's efforts to read sense into the claims are commendable during examination, when the meanings of the column and row designations may be clarified and ambiguities resolved on the record. *On appeal*, however, such attempted clarifications *by the Examiner* are misguided. As the Federal Circuit observed in a related context,

> [s]uch an approach puts the burden in the wrong place. It is the applicants' burden to precisely define the invention, not the PTO's. *See* 35 U.S.C. § 112 ¶ 2 ("The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.").

In re Morris, 127 F.3d 1048, 1056 (Fed. Cir. 1997). On appeal, the Examiner's role is to explain why the claims are indefinite, and Appellants' role is to explain why the Examiner is in error.

Having found claims 9 and 10 to be indefinite—i.e., the scope and content of the claims could not be determined with reasonable certainty—the Examiner properly withdrew them from consideration as against the prior art. (FR 4.) *Cf. In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970); *In re Steele*, 305 F.2d 859, 862-63 (CCPA 1962) (instructing that claims that are indefinite cannot be held obvious).[5]

We turn now to the rejections over prior art. The Examiner cited specific figures and descriptive paragraphs in Clarkson as evidence supporting anticipation and obviousness. (FR 4-7.) We note further that the Examiner determined that the subject matter covered by claims 5 and 6 was neither anticipated nor obvious over the prior art of record. (FR 7.) Chan's response is a blanket denial that shared vias and the combinations of limitations set out in the claims are described by Clarkson. (Br. 5.) Such an "argument," at most, points out what the claims recite. However, the

[5] In the analysis for definiteness, the Examiner's consideration of the alleged problem of what row and column "should be" specified is misguided, absent evidence in the record that the Applicant is attempting to interpret the claims in a manner inconsistent with the plain language of the claims, informed by any special definitions in the Specification or generally accepted in the art. If, unlike in claims 9 and 10, the contact pads could be in the specified column and row, the claim is definite. Whether the claimed subject matter corresponds to what is described in the specification is not a problem of definiteness, but one of whether the written description requirement of 35 U.S.C. § 112, first paragraph has been satisfied. That issue, however, has not been placed before us in this appeal.

regulations governing appeals specifically states that "[a] statement which merely points out what a claim recites will not be considered an argument for separate patentability of the claim." 37 C.F.R. § 41.37(c)(1)(vii) (2009), last sentence. Indeed, such a statement amounts to no more than pleading. It is an invitation to the Board to take up the Appellants' burden to point out where the Examiner erred. In some cases, particularly with simple claims with clearly defined terms, and a simple reference, the distinction might lapse to mere formalism. This case, however, is not so simple, and the record shows that the Examiner considered the evidence and the claim limitations carefully. On this record, we decline Chan's invitation to carry Appellants' burden. We conclude that Chan has failed to show harmful error in the Examiner's findings of fact as to anticipation of claims 1-4 by Clarkson. As Chan's arguments against the obviousness rejection rely solely on the arguments against anticipation, we conclude that Chan has failed to show harmful error in the obviousness rejection.

D. Order

We AFFIRM the rejection of claims 9 and 10 under 35 U.S.C. § 112(2).

We AFFIRM the rejection of claims 1-4 under 35 U.S.C. § 102(e) in view of the teachings of Clarkson.

We AFFIRM the rejection of claims 11 and 12 under 35 U.S.C. § 103(a) in view of the teachings of Clarkson.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

Ssl

KRAMER & AMADO, P.C.
SUITE 240
1725 DUKE STREET
ALEXANDRIA, VA 22314